IN THE CLAIMS

Please amend the claims as follows:

Claims 1-2 (Canceled).

Claim 3 (Currently Amended): A serial transmission path switching system comprising:

a switch section having a plurality of input lines and a plurality of output lines to perform line-switching between the input lines and output lines;

a plurality of first serial transmission paths connected to the input lines, respectively;

input buffers connected to input-side communication devices and terminals of the first serial transmission paths, respectively, to equalize transmission signals from said input-side communication devices and send the signals to the first serial transmission paths;

a plurality of second serial transmission paths connected to the output lines, respectively;

output buffers connected to output-side communication devices and terminals of the second serial transmission paths, respectively, to equalize transmission signals from the second serial transmission paths and send the signals to said output-side communication devices;

a receiving section inserted between the first serial transmission paths and the input lines to receive the transmission signals from the first serial transmission paths and supply the signals to the input lines; and

a transmitting section inserted between the output lines and the second serial transmission paths to receive the transmission signals from the output lines and supply the signals to the second serial transmission paths, wherein

said receiving section and said transmitting section comprise an optical receiving section and an optical transmitting section, respectively, and transmission paths of the first and second serial transmission paths, connected to said optical receiving section and said optical transmitting section, comprise optical fiber cables.

Claim 4 (Canceled).

Claim 5 (Currently Amended): The system according to claim 3 [[4]], wherein buffers of said input and output buffers, connected to said optical fiber cables, have a function of converting an optical signal into an electrical signal or vice versa.

Claims 6-8 (Canceled).

Claim 9 (Previously Presented): A serial transmission path switching system comprising:

a switch section having a plurality of input lines and a plurality of output lines to perform line-switching between the input lines and output lines;

a plurality of first serial transmission paths connected to the input lines, respectively;

input buffers connected to input-side communication devices and terminals of the first serial transmission paths, respectively, to equalize transmission signals from said input-side communication devices and send the signals to the first serial transmission paths;

a plurality of second serial transmission paths connected to the output lines, respectively; and

output buffers connected to output-side communication devices and terminals of the second serial transmission paths, respectively, to equalize transmission signals from the

second serial transmission paths and send the signals to said output-side communication devices,

wherein said switch section comprises:

a switch having a plurality of input portions and a plurality of output portions to perform line-switching between said input portions and output portions,

frequency band expanding members connected to said output portions, respectively, to increase a gain of high-frequency-side frequency characteristics of each of transmission signal from said output portions, and

buffer amplifiers connected to said frequency band expanding members to buffer the transmission signals from said frequency band expanding members and send the signals to the output lines, respectively.

Claim 10 (Original): The system according to claim 9, wherein said frequency band expanding member comprises a high-pass filter.

Claim 11 (Original): The system according to claim 10, wherein said high-pass filter comprises a resister and a capacitor which are connected in parallel.

Claim 12 (Previously Presented): A serial transmission path switching system comprising:

a switch section having a plurality of input lines and a plurality of output lines to perform line-switching between the input lines and output lines;

a plurality of first serial transmission paths connected to the input lines, respectively;

input buffers connected to input-side communication devices and terminals of the first serial transmission paths, respectively, to equalize transmission signals from said input-side communication devices and send the signals to the first serial transmission paths;

a plurality of second serial transmission paths connected to the output lines, respectively; and

output buffers connected to output-side communication devices and terminals of the second serial transmission paths, respectively, to equalize transmission signals from the second serial transmission paths and send the signals to said output-side communication devices,

wherein said switch section comprises:

a switch having a plurality of input portions and a plurality of output portions to perform line-switching between said input portions and output portions,

conversion members connected to said output portions to convert transmission signals from said output portions into pairs of positive and negative differential signals, respectively,

pairs of frequency band expanding members connected to said conversion members, respectively, to increase a gain of high-frequency-side frequency characteristics of each of the positive and negative differential signals from said conversion members, and

buffer amplifiers connected to said pairs of frequency band expanding members to combine the transmission signals from the pairs of frequency band expanding members into single signals, buffer the single signals and send the signals to the output lines, respectively.

Claim 13 (Original): The system according to claim 12, wherein said frequency band expanding member comprises a high-pass filter.

Claim 14 (Original): The system according to claim 13, wherein said high-pass filter comprises a resister and a capacitor which are connected in parallel.

Claim 15 (Previously Presented): A serial transmission path switching system comprising:

a switch section having a plurality of input lines and a plurality of output lines to perform line-switching between the input lines and output lines;

a plurality of first serial transmission paths connected to the input lines, respectively;

input buffers connected to input-side communication devices and terminals of the first serial transmission paths, respectively, to equalize transmission signals from said input-side communication devices and send the signals to the first serial transmission paths;

a plurality of second serial transmission paths connected to the output lines, respectively; and

output buffers connected to output-side communication devices and terminals of the second serial transmission paths, respectively, to equalize transmission signals from the second serial transmission paths and send the signals to said output-side communication devices,

wherein said switch section comprises:

a switch having a plurality of input portions and a plurality of output portions to perform line-switching between said input portions and output portions, and

buffer amplifiers connected to said output portions to buffer transmission signals from said output portions and send the signals to the output lines, respectively, and

wherein an operation speed of said switch is set to be not less than 100 times a bit rate of a digital signal to be input to said input portion.

Claim 16 (Currently Amended): ~~The system according to claim 3~~ A serial transmission path switching system comprising:

a switch section having a plurality of input lines and a plurality of output lines to perform line-switching between the input lines and output lines;

a plurality of first serial transmission paths connected to the input lines, respectively;

input buffers connected to input-side communication devices and terminals of the first serial transmission paths, respectively, to equalize transmission signals from said input-side communication devices and send the signals to the first serial transmission paths;

a plurality of second serial transmission paths connected to the output lines, respectively;

output buffers connected to output-side communication devices and terminals of the second serial transmission paths, respectively, to equalize transmission signals from the second serial transmission paths and send the signals to said output-side communication devices;

a receiving section inserted between the first serial transmission paths and the input lines to receive the transmission signals from the first serial transmission paths and supply the signals to the input lines; and

a transmitting section inserted between the output lines and the second serial transmission paths to receive the transmission signals from the output lines and supply the signals to the second serial transmission paths, wherein

(a) said receiving section has Li (Li is a natural number) distributors for distributing digital signals of Li channels to a first group and a second group in units of a channel,

(b) said switch section comprises:

an input stage formed by parallelly arranging a plurality of switches and having a total of at least 2Li (Li is a natural number) inputs, each switch having a maximum number N (N is a natural number) of inputs and a maximum number M (M is a natural number) of outputs,

an output stage formed by parallelly arranging a plurality of switches and having a total of at least 2Lo (Lo is a natural number) outputs, each switch having the maximum number N of inputs and the maximum number M of outputs, and

a middle stage inserted between said input stage and said output stage and formed by parallelly arranging (P + Q) where P (P is a natural number) is the number of inputs of one switch of said input stage for one of said groups, and Q (Q is a natural number) is the number of outputs of one switch of said output stage for one of said groups switches having inputs equal in number to the total number of outputs of said switches of said input stage and outputs equal in number to the total number of inputs of said switches of said output stage,

wherein the digital signals of said first and second groups of each of the Li channels, which are distributed by said receiving section, are input to switches of said input stage different from each other between said groups, passed through said plurality of switches of said middle stage, and output from switches of said output stage different form each other between said groups, and

(c) said transmitting section has Lo selectors such that the digital signals of said first and second groups, which are output from switches of said switch section different from each other between said groups, are input to corresponding selectors, and the digital signal of one of said groups is selectively output.

Claim 17 (Original): The system according to claim 16, wherein the number of switches of said input stage is (2Li/N), and the number of switches of said output stage is

(2Lo/M).

Claim 18 (Original): The system according to claim 16, wherein the digital signals of said first group are input to N/2 lines of one switch of said input stage, and the digital signals of said second group of channels different from those of said first group are input to N/2 remaining lines.

Claim 19 (Original): The system according to claim 16, wherein a plurality of output lines of one switch of said input stage are connected to input lines of different switches of said middle stage, respectively, and a plurality of input lines of one switch of said output stage are connected to output lines of different switches of said middle stage, respectively.

Claim 20 (Original): The system according to claim 16, wherein a plurality of switches of said input stage are combined to form one switch module, and a plurality of switches of said output stage are combined to form one switch module such that the maximum number of inputs and the maximum number of outputs of one switch of each of said input stage and said output stage equals the maximum number of inputs and the maximum number of outputs of one switch of said middle stage.

Claim 21 (Previously Presented): The system according to claim 9, further comprising:

a receiving section inserted between the first serial transmission paths and the input lines to receive the transmission signals from the first serial transmission paths and supply the signals to the input lines.

Claim 22 (Previously Presented): The system according to claim 21, further comprising:

a transmitting section inserted between the output lines and the second serial transmission paths to receive the transmission signals from the output lines and supply the signals to the second serial transmission paths.

Claim 23 (Previously Presented): The system according to claim 22, wherein said receiving section and said transmitting section comprise an optical receiving section and an optical transmitting section, respectively, and transmission paths of the first and second serial transmission paths, connected to said optical receiving section and said optical transmitting section, comprise optical fiber cables.

Claim 24 (Previously Presented): The system according to claim 23, wherein buffers of said input and output buffers, connected to said optical fiber cables, have a function of converting an optical signal into an electrical signal or vice versa.

Claim 25 (Previously Presented): The system according to Claim 9, wherein said input buffers comprise a buffer designed to be compatible with different transfer rates, and said output buffers comprise a buffer designed to be compatible with different transfer rates.

Claim 26 (Previously Presented): The system according to Claim 9, wherein said input and output buffers comprise a buffer designed to be compatible with a plurality of transfer rates and having a function of selectively setting a transmission rate in accordance with a connected communication device.

Claim 27 (New): The system according to Claim 9, wherein said switch section comprises a matrix switch section having a plurality of switch arrayed in a matrix format.